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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,482	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,11 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5,11 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Applicant's amendment of claim 3, cancellation of claim 13 and the addition of claims 14-19 in the response dated 8/7/2007 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Therefore, the non-doped polysilicon body being etched from a non-doped region of the polysilicon layer wherein an endpoint of the etch is based on the etching of the non-doped polysilicon body of claims 3 and 15 must be shown or the feature(s) canceled from the claim(s). Fig. 3(c) shows no indication that the polysilicon body is etched, which would be an essential feature of the invention given by claims 3 and 15 due to the limitation that the endpoint of the etch is based on the etching of the non-doped polysilicon portion.

Further the non-doped polysilicon body occupying an area that is smaller than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode must be shown or the feature(s) canceled from the claim(s). Fig. 3(c) shows the non-doped polysilicon body being clearly larger than the total area of the N and P type gates.

No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liau et al. (U.S. Patent # 5783850) (previously of record (PTO-892 of 5/17/2006)) in view of Gabriel et al. (U.S. Patent # 6541359) with evidence provided by Lu (U.S. Patent # 4989057).

Regarding claim 15, Liau et al. discloses a dry etching method for a semiconductor device, comprising the following steps of:

implanting a first region of a polysilicon layer 26 with N type ions (Col. 4, Lines 25-40), the first region having a first area (see Fig. 4);

implanting a second region of the polysilicon layer 26 with P type ions (right-most region of Fig. 7), the second region having a second area (see Fig. 7) (Col. 4, Lines 25-50); and

forming an N type polysilicon gate electrode 41 from the first region (see middle region of Fig. 7), a P type polysilicon gate electrode 41 from the second region (right-most region of Fig. 7), and a non-doped polysilicon body 40 from a non-doped region of the polysilicon layer (left-most region of Fig. 7), the N type polysilicon gate electrode occupying an area that is smaller than the first area (see Fig. 7), the P type polysilicon gate electrode occupying an area that is smaller than the second area (see Fig. 7).

Liau et al., however, fails to disclose the gate electrode and the undoped polysilicon body being simultaneously etched during an etching process wherein the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon body or wherein the non-doped polysilicon body occupies an area that is smaller than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode.

Gabriel et al. teaches simultaneously gate-etching (Gabriel et al., Col. 7, Lines 6-9) an N type polysilicon gate electrode (Gabriel et al., Fig. 5A (540, 550)), a P type

polysilicon gate electrode (Gabriel et al., Fig. 5A (540, 550)) (Gabriel et al., Col. 6, Line 62 – Col. 7, Line 9), and a non-doped polysilicon body (Col. 7, Lines 1-9) during an etching process wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped polysilicon body (Col. 7, Lines 6-9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the simultaneous gate etching process of Gabriel et al. into the device of Liau et al. The ordinary artisan would have been motivated to modify Liau et al. in the above manner for the purpose of avoiding microtrenching (Gabriel et al., Col. 2, Lines 35-45) while providing a strong detectable endpoint signal (Gabriel et al., Col. 7, Lines 1-10).

Liau et al. and Gabriel et al., however, fail to disclose wherein the non-doped polysilicon body occupies an area that is smaller than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode.

It would have been obvious to one of ordinary skill in the art to modify the size of the undoped polysilicon portion of Liau et al. and Gabriel et al. As is taught by Lu, the gate length/channel length of the transistor formed using the undoped portion of polysilicon in the gate is proportional to the breakdown voltage and holding voltage parameters of the device (Lu, Col. 7, Lines 40-55). Therefore, said gate length/channel length is considered to be a result effective variable where the result is the modification of the breakdown and holding voltage levels of the semiconductor device. The claim to a change in the size of the undoped portion of the polysilicon layer therefore constitutes

an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Regarding claim 16, Liau et al. and Gabriel et al. (with evidence provided by Lu) disclose the dry etching method according to claim 15, wherein the nondoped polysilicon body is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Regarding claim 17, Liau et al. and Gabriel et al. (with evidence provided by Lu) disclose the dry etching method according to claim 15, wherein the P type polysilicon gate electrode is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

4. Claims 3, 5, 11, 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liau et al. (U.S. Patent # 5783850) in view of Gabriel et al. (U.S. Patent # 6541359) further in view of Lee et al. (U.S. Patent # 5665203) with evidence provided by Lu (U.S. Patent # 4989057).

Regarding claims 3, 5, 18 and 19, Liau et al. and Gabriel et al. disclose the dry etching method (Gabriel et al., Col. 1, Lines 34-38) of claim 15, wherein the etching process includes a stage using a mixed gas of HBr and O_2 (Gabriel et al., Col. 1, Lines 63-65), but fail to disclose the etching process being a two step etching process wherein a second stage of the etch uses a mixed gas of HBr, O_2, and He.

Lee et al. teaches a similar method wherein the gate etching process is a two-step process which uses a first stage atmosphere of HBr, Cl_2 and He and a second stage atmosphere of HBr, 0_2 and He (Lee et al., Col. 2, lines 39-41).

It would have been obvious to one of ordinary skill in the art to incorporate the method of Lee et al. into the method of Liau et al. and Gabriel et al. The ordinary artisan would have been motivated to modify Liau et al. and Gabriel et al. in the above manner for the purpose of forming perfectly vertical gate sidewalls (Lee et al. Col. 2, Lines 23-28).

Regarding claim 11, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 3, wherein the P type polysilicon gate electrode is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Regarding claim 14, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 3, wherein the nondoped polysilicon body is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Response to Arguments

5. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK
10/15/07

EUGENE LEE
PRIMARY EXAMINER